

08207

FIG. 1

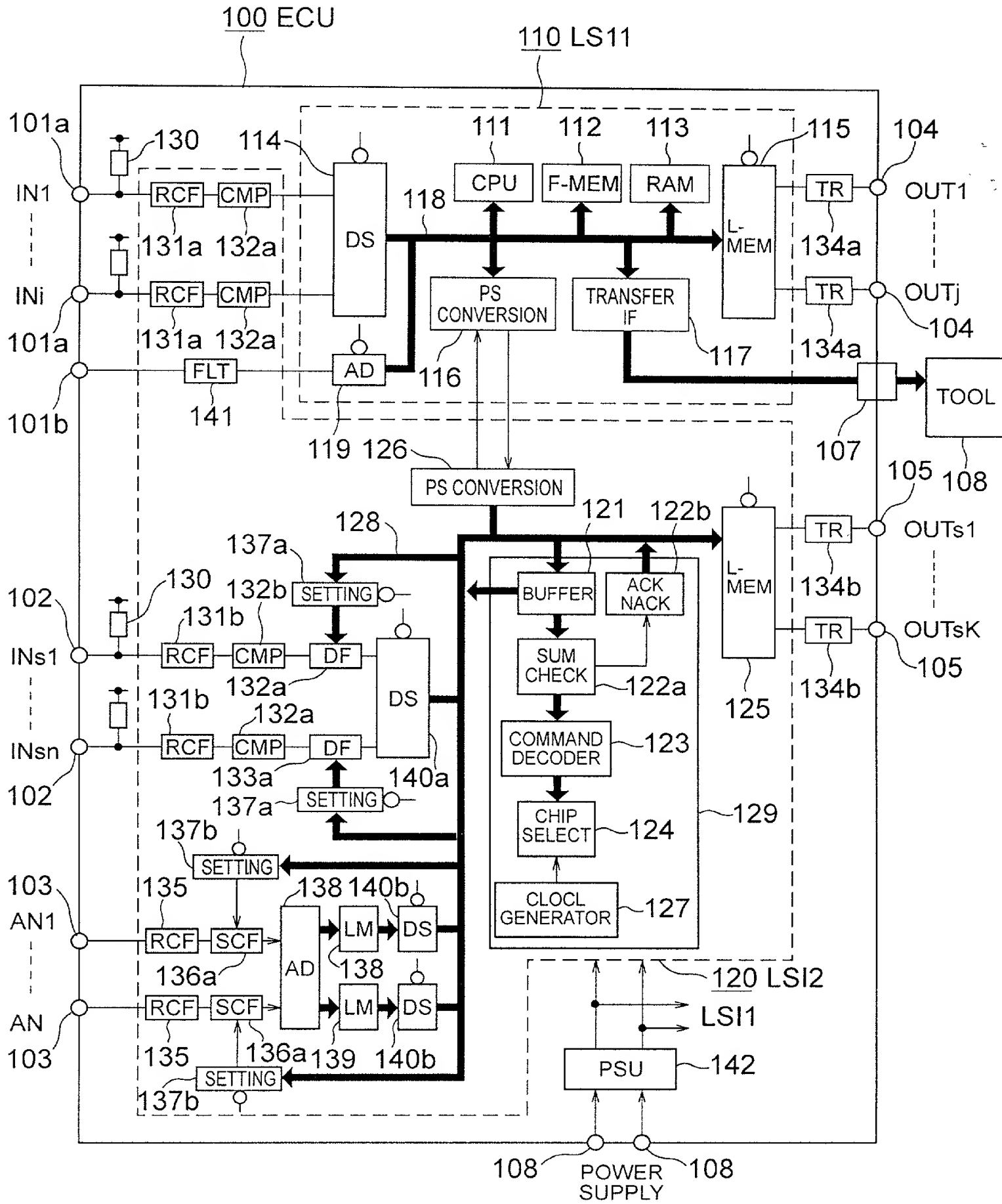
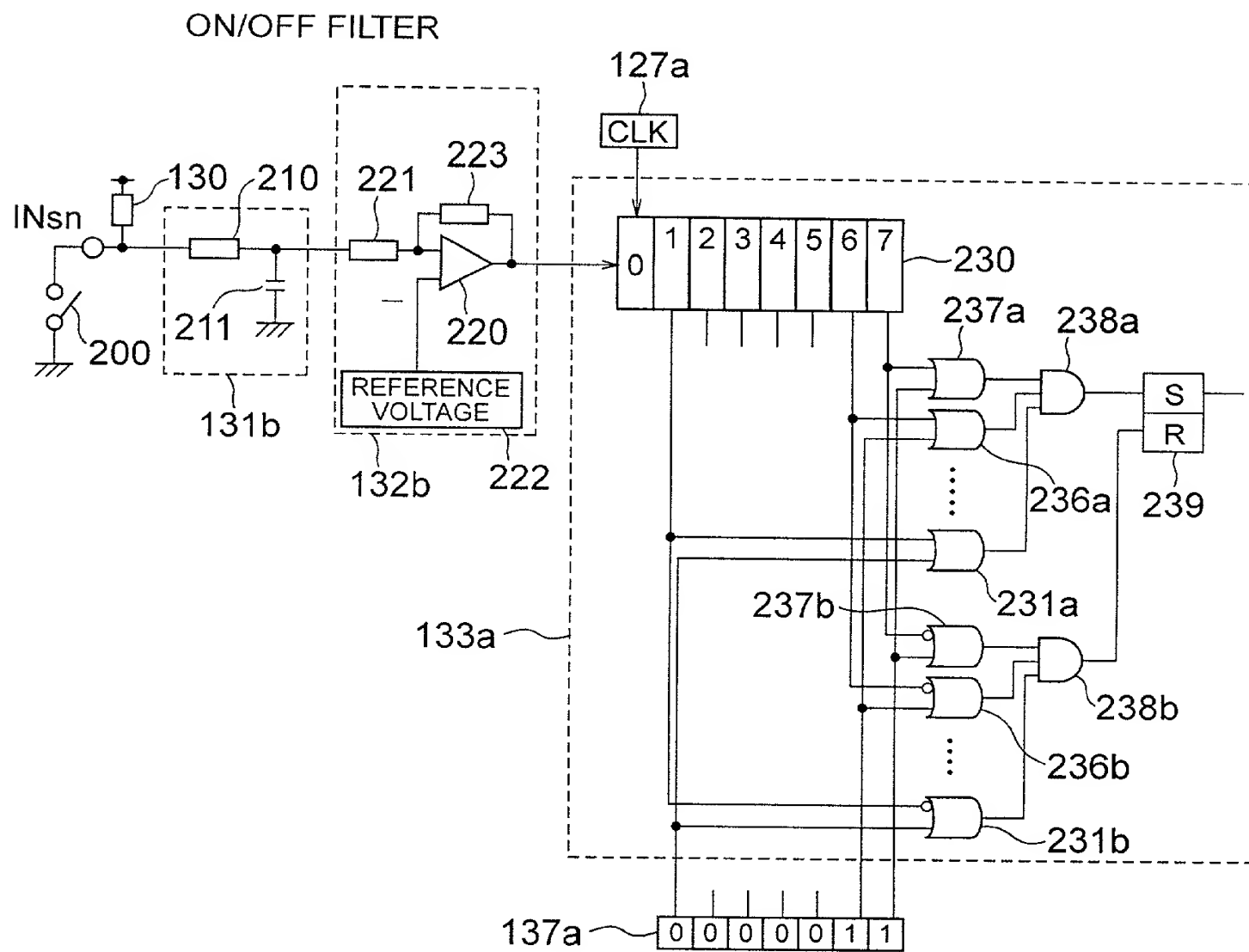


FIG. 2



[illegible]

FIG. 4A

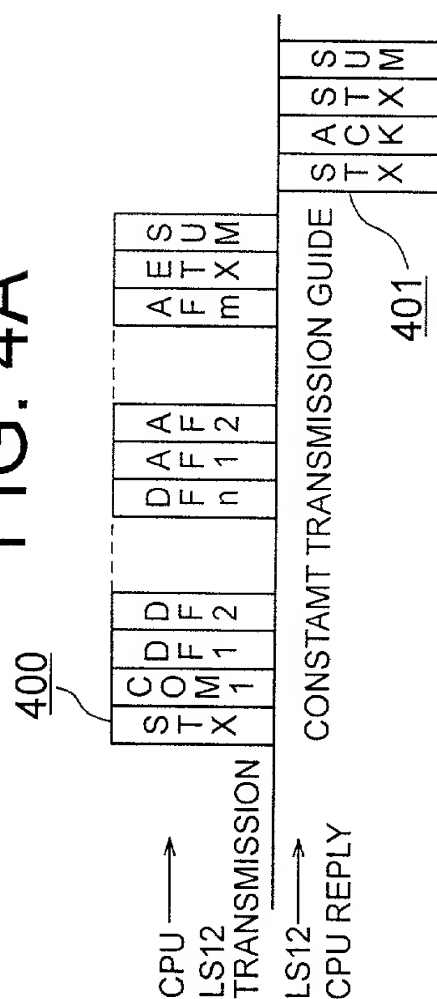


FIG. 4B

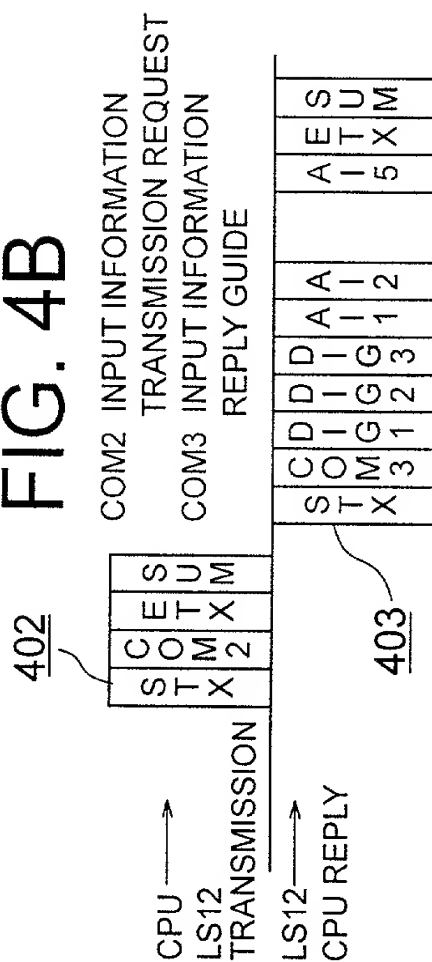


FIG. 4C

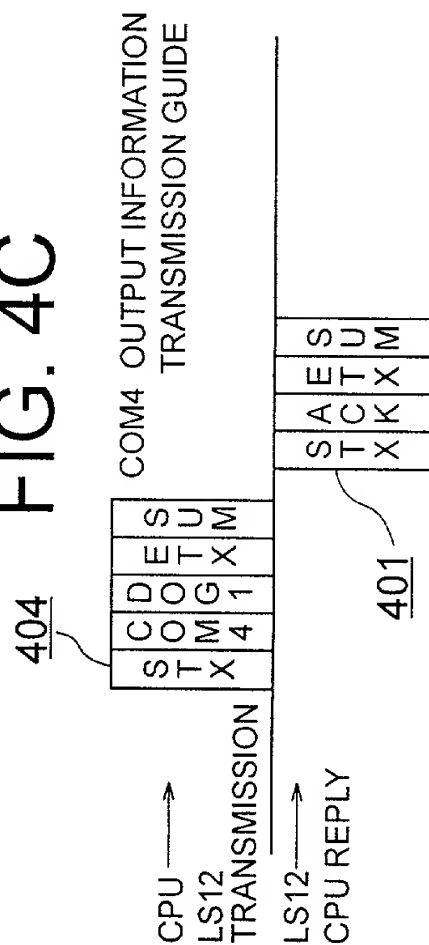


FIG. 4D

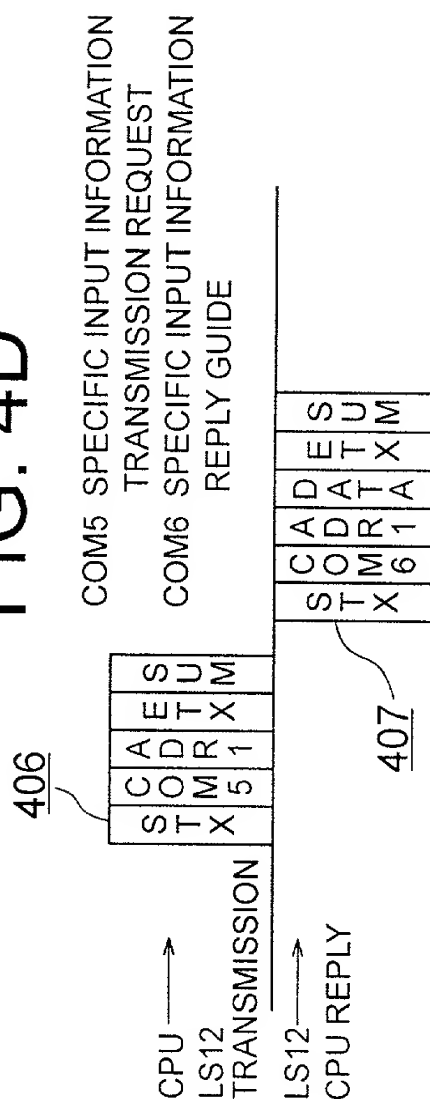


FIG. 4E

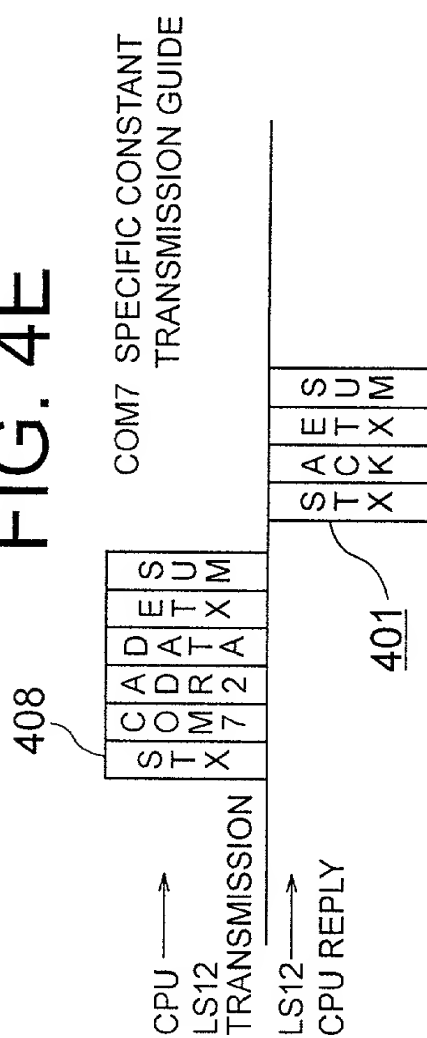


FIG. 4F

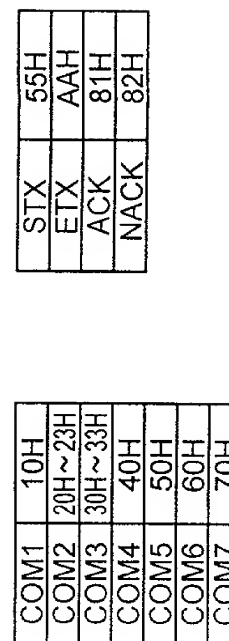
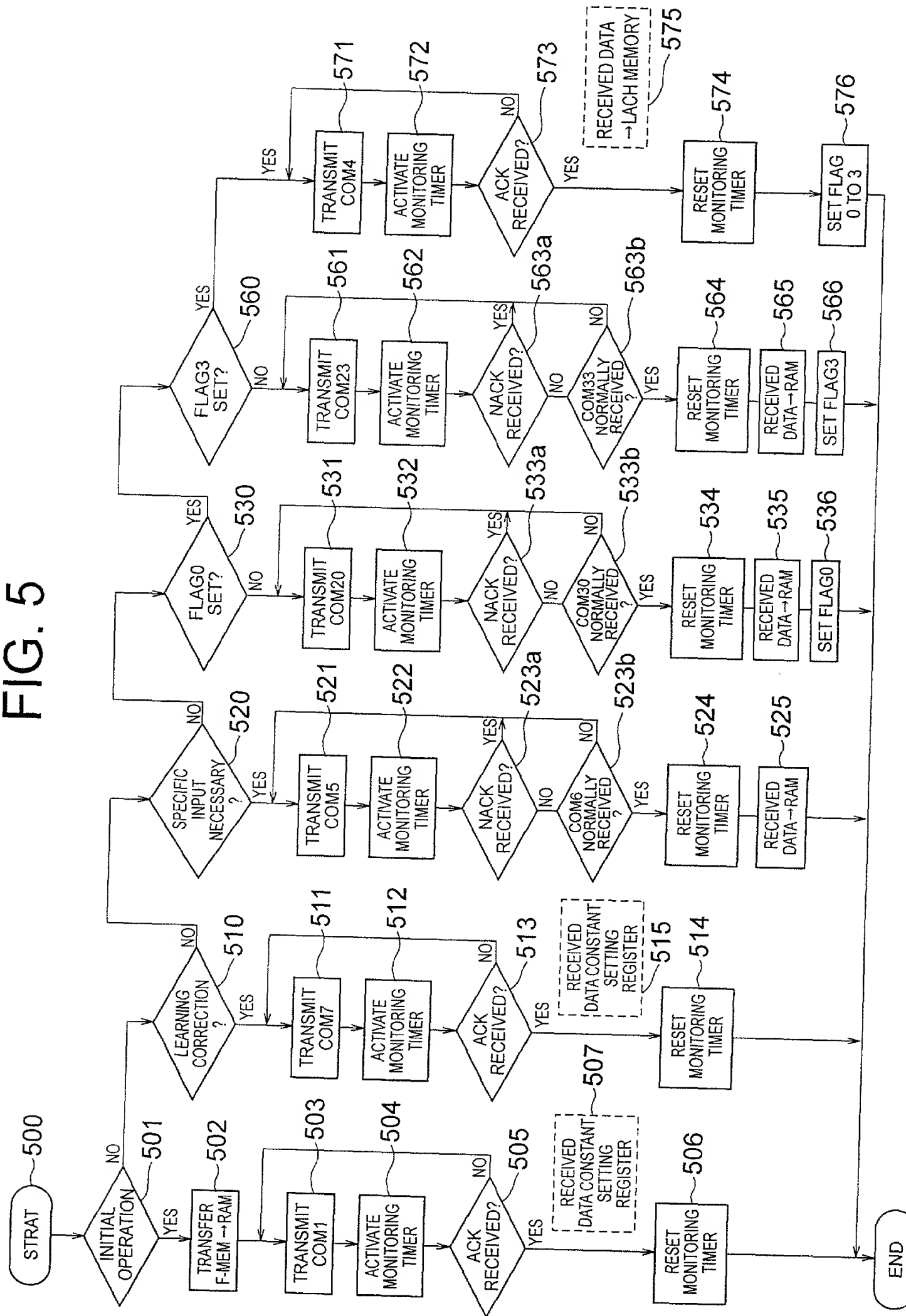
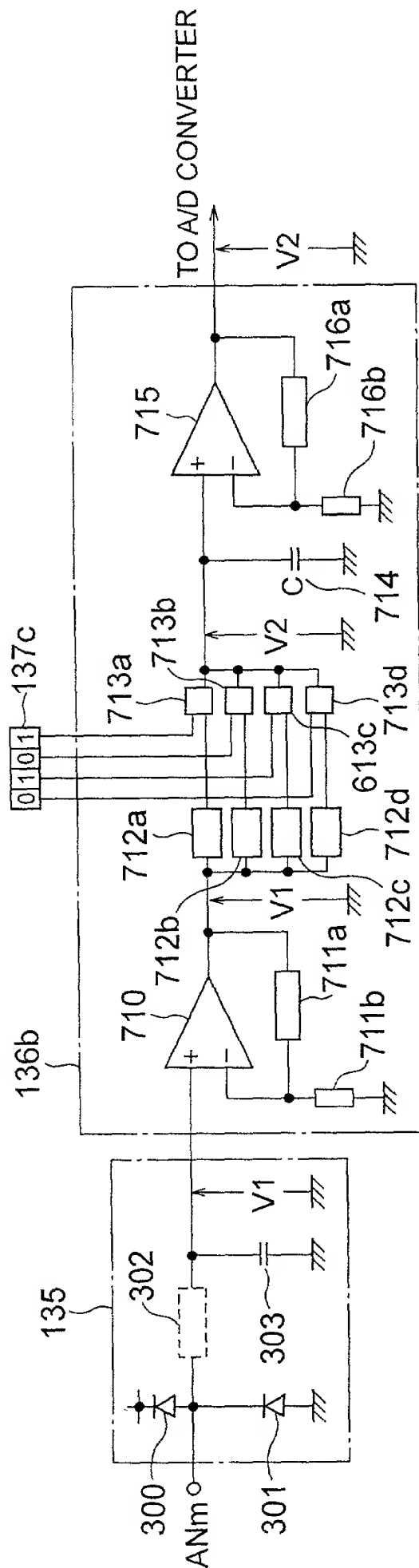


FIG. 5



The diagram illustrates a digital-to-analog converter (DAC) circuit. It starts with an input signal  $IN_{sn}$  connected to a resistor 130. The output of resistor 130 is connected to a resistor 210, which is in series with a capacitor 211 connected to ground. This combination is part of a block 131b. The output of resistor 210 is connected to a resistor 221, which is in series with a comparator 220. The comparator 220 has a non-inverting input connected to a reference voltage source 222 and an inverting input connected to the output of resistor 221. The output of the comparator 220 is connected to a resistor 223, which is in series with a resistor 132b. This combination is part of a block 132b. The output of resistor 223 is connected to a resistor 133b, which is in series with a clock signal  $CLK$ . This combination is part of a block 133b. The output of resistor 133b is connected to a logic block 600a. The logic block 600a has a clock input  $CLK$  and a data input  $Q$ . The output of logic block 600a is connected to a logic block 600b. The logic block 600b has a clock input  $CLK$  and a data input  $P$ . The output of logic block 600b is connected to a logic block 601. The logic block 601 has a clock input  $CLK$  and a data input  $UP$ . The output of logic block 601 is connected to a logic block 602. The logic block 602 has a clock input  $CLK$  and a data input  $DN$ . The output of logic block 602 is connected to a logic block 603a. The logic block 603a has a clock input  $CLK$  and a data input  $SET$ . The output of logic block 603a is connected to a logic block 603b. The logic block 603b has a clock input  $CLK$  and a data input  $CURRENT$ . The output of logic block 603b is connected to a logic block 604a. The logic block 604a has a clock input  $CLK$  and a data input  $Q$ . The output of logic block 604a is connected to a logic block 604b. The logic block 604b has a clock input  $CLK$  and a data input  $P$ . The output of logic block 604b is connected to a logic block 605. The logic block 605 has a clock input  $CLK$  and a data input  $S$ . The output of logic block 605 is connected to a digital-to-analog converter  $DS$ .

FIG. 7



E.G. 8

